PART NO. 0112-0278-10

K100-D/488
GPIB Analyzer

OPERATING AND SERVICE MANUAL

GOULD
Electronics

OPERATING AND SERVICE MANUAL

MODEL K100-D/488 GPIB ANALYZER

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SECTION I

GENERAL INFORMATION

1.1 Certification

Gould Inc. certifies that this instrument was thoroughly tested and inspected and found to meet its published specifications when it was shipped from the factory.

1.2 Warranty

All Gould Inc. products are warranted against defects in materials and workmanship. This warranty applies for one year from the date of delivery, or, in the case of certain major components listed in the operating manual, for the specified period. We will repair or replace products that prove to be defective during the warranty period. If a unit fails within thirty days of delivery, Gould Inc. will pay all shipping charges relating to the repair of the unit. Units under warranty, but beyond the thirty day period, should be sent to Gould Inc. prepaid and Gould Inc. will return the unit prepaid. Units out of the one year warranty period, the customer will pay all freight charges. IN THE EVENT OF A BREACH OF GOULD INC.'S WARRANTY, GOULD INC. SHALL HAVE THE RIGHT IN ITS DISCRETION EITHER TO REPLACE OR REPAIR THE DEFECTIVE GOODS OR TO REFUND THE PORTION OF THE PURCHASE PRICE APPLICABLE THERETO. THERE SHALL BE NO OTHER REMEDY FOR BREACH OF THE WARRANTY. IN NO EVENT SHALL GOULD INC. BE LIABLE FOR THE COST OF PROCESSING, LOST PROFITS, INJURY TO GOODWILL, OR ANY SPECIAL OR CONSEQUENTIAL DAMAGES. THE FOREGOING WARRANTY IS EXCLUSIVE OF ALL OTHER WARRANTIES, WHETHER EXPRESSED OR IMPLIED, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

1.3 Description

The Model K100-D/488 GPIB Analyzer was designed to provide a convenient and effective method for the digital designer and troubleshooter to utilize the Model K100-D Logic Analyzer when the task involves the design or troubleshooting of a GPIB (IEEE-488) system or interface. Compact and simple to use, this probing accessory allows monitoring of bi-directional data flows and isolation of timing problems. The K100-D/488 transforms the K100-D into a high resolution GPIB analyzer.

As shown in Figure 1.1, the pod replaces the standard probes as the input to the K100-D via the front panel connectors. A 24 pin GPIB compatible "piggy-back" type cable terminating on a 36" ribbon cable provides connection between the pod and the GPIB.

GPIB data lines (DIO1-8) are input via the 488 INPUT connector and are recorded on channels 0 to 7 of the K100-D. The handshake and management lines are input via the 488 INPUT and recorded on channels 8 to F (INPUT B) of the K100-D. The CK (Clock) input to the K100-D is tied to the DAV line of the bus and the CQ (Clock Qualifier) is tied to +5V (TTL true). Lines 8-F, CK or CQ may be switched and thus disconnected from their origins, and to a new origin selected by the user (see Figure 1.3). The user selected inputs enter the pod via a 20-pin connector labeled Input A (gray). The 20-pin connector has a ribbon cable terminated by 0.25"

diameter wire wrap receptacles. Grabbers are included with a K100-D/488 that are fitted to the wire wrap receptacles, to allow incircuit probing. The wire wrap receptacles can be used in conjunction with 0.25" wire wrap posts or DIP clips. The cover of the pod includes a power "ON" indicator LED (green) and 10 two-position switches (see Figure 1.2).

The numbering, 1 to 5, under the switches has no meaning to the user. For convenience, all user inputs are labeled at the wire wrap receptacles. The labels correspond to the K100-D channels on which the user inputs will be recorded.

When all the switches are in the GPIB INPUT positions, the pod maintains a transparent relationship with the bus. The user inputs are terminated by one TTL load (74LS244 chip).

1.4 Specification

DESCRIPTION

The K100-D/488 allows convenient and flexible connection of the K100-D to the GPIB bus. All 16 bus signals may be recorded at internal clock rates up to 100 MHz (10 ns/sample). The bus signal DAV may be used to clock the data when timing information is not required. Eight additional USER INPUTS are provided to allow probing other signals. External Clock (CK) and Clock Qualifier (CQ) inputs are also provided.

INPUTS

Impedance:	Low power Schottkey TTL input I_{IL} max = 0.2 μA (all inputs)
Capacitance:	30 pF max

GPIB INPUT

16 inputs all GPIB signals are recorded.
8 DIO lines are always monitored and recorded on channels 0-7 of the K100-D.
8 management/handshake lines may be selectively recorded on channels 8-F of the K100-D.
26 pin card-edge connector (0.1" centers).
A 36" cable and connector which mates with standard GPIB connectors is provided.

USER INPUTS

8 data inputs may be monitored and recorded on channels 8-F of the K100-D.
1 Clock input (CK) ANDed with 1 Clock Qualifier input (CQ).
20 pin card edge (0.1" centers).
A 24" cable is provided for connection to 0.025" sq. posts.

EXT. CLOCK TIMING SPECIFICATION

Max external clock rate = 10 MHz.

Set-up Time = 20 ns max.
Hold Time = 20 ns max.

INPUT SELECTION

8 switches on the front panel allow individual selection of either the GPIB's management/ handshake lines or USER INPUTS for recording on channels 8-F of the K100-D.

1 switch allows external clock selection of either DAV or USER CL (Clock). The K100-D may alternately use it's own internal clock.

1 switch allows input of a USER CQ (Clock Qualifier) which may be used with either external clock selected above.

Temp. Range:	0-50^{o} C operating.
Size:	9.2 cm (3.6") wide, 17.3 cm (6.8") deep, 2.5 cm (1.0") thick.
Weight:	0.5 kg (1.0 lb.).
Power:	Provided by K100-D (rear panel) through a 3-conductor cable with LEMO connector.
Power Consumption:	+5.0 V @ 250 mA -5.2 V @ 350 mA.

Accessories Included: Each K100-D/488 is shipped complete with one GPIB Input cable, one User Input cable, and an Operating and Service Manual.

Accessories Available: For your convenience in meeting spare and multiple requirements, the following items listed below can be purchased separately.

BIOMATION PART NUMBER	ITEM
PN 0112-0274	GPIB Input cable (36")
PN 0112-0365	User Input cable (24")
PN 0112-0333	Spare grabbers for K100-D (Qty. 20)
PN 0112-0278	Extra Operating and Service Manual

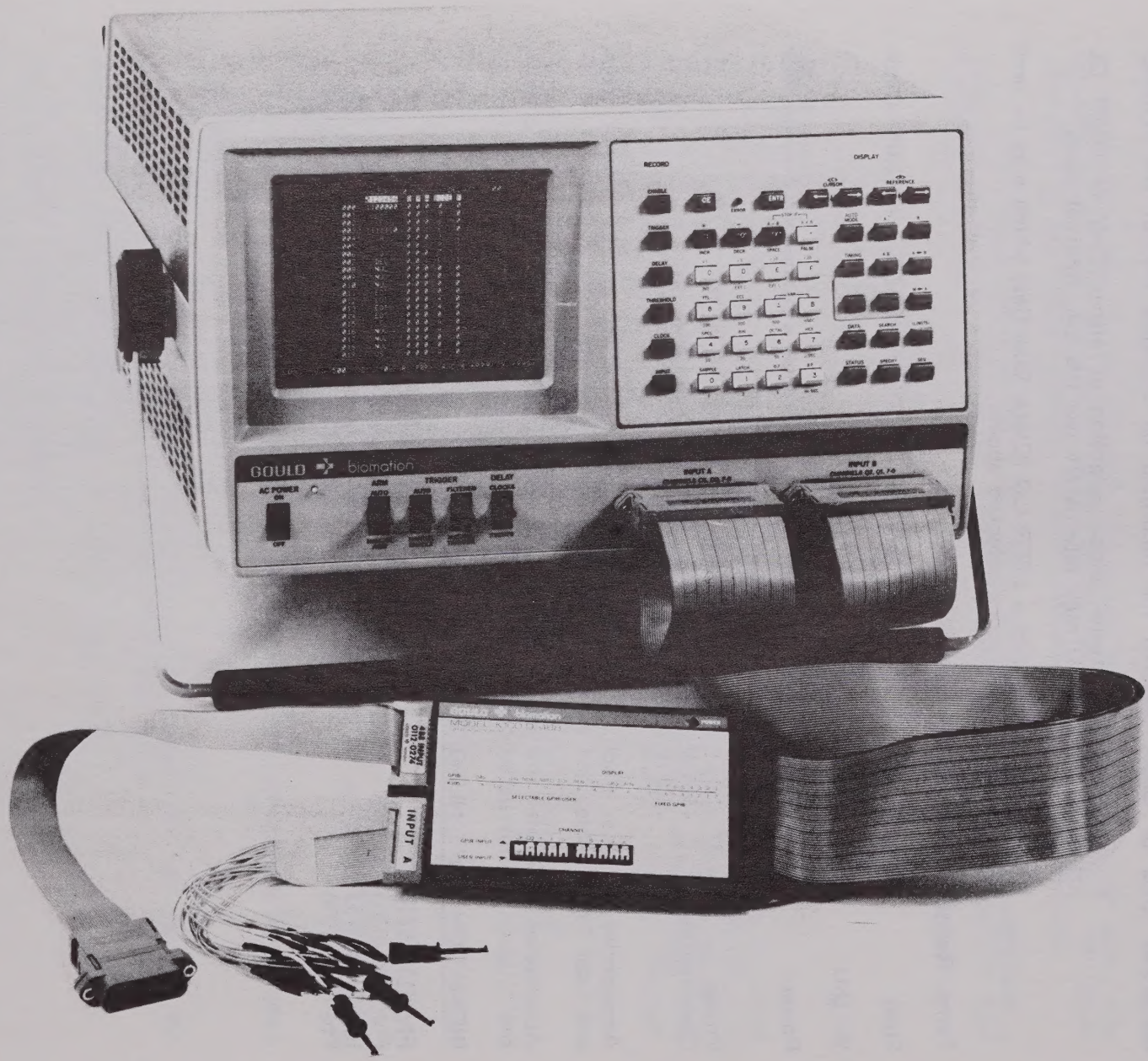

Figure 1.1 The K100-D Logic Analyzer with K100-D/488 GPIB Analyzer installed.

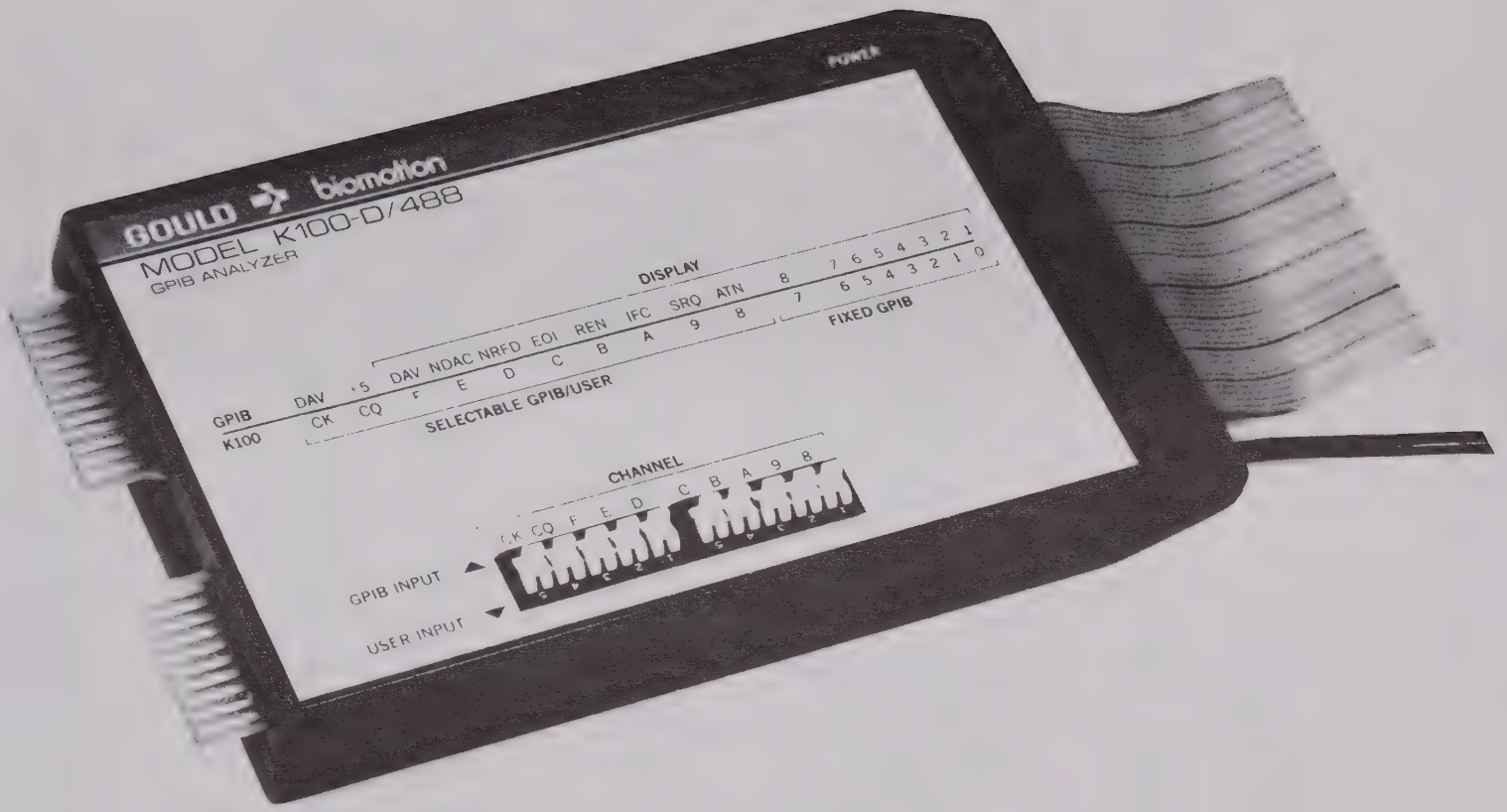

Figure 1.2 Front panel view of the K100-D/488 GPIB Analyzer. All inputs are in GPIB switch positions.

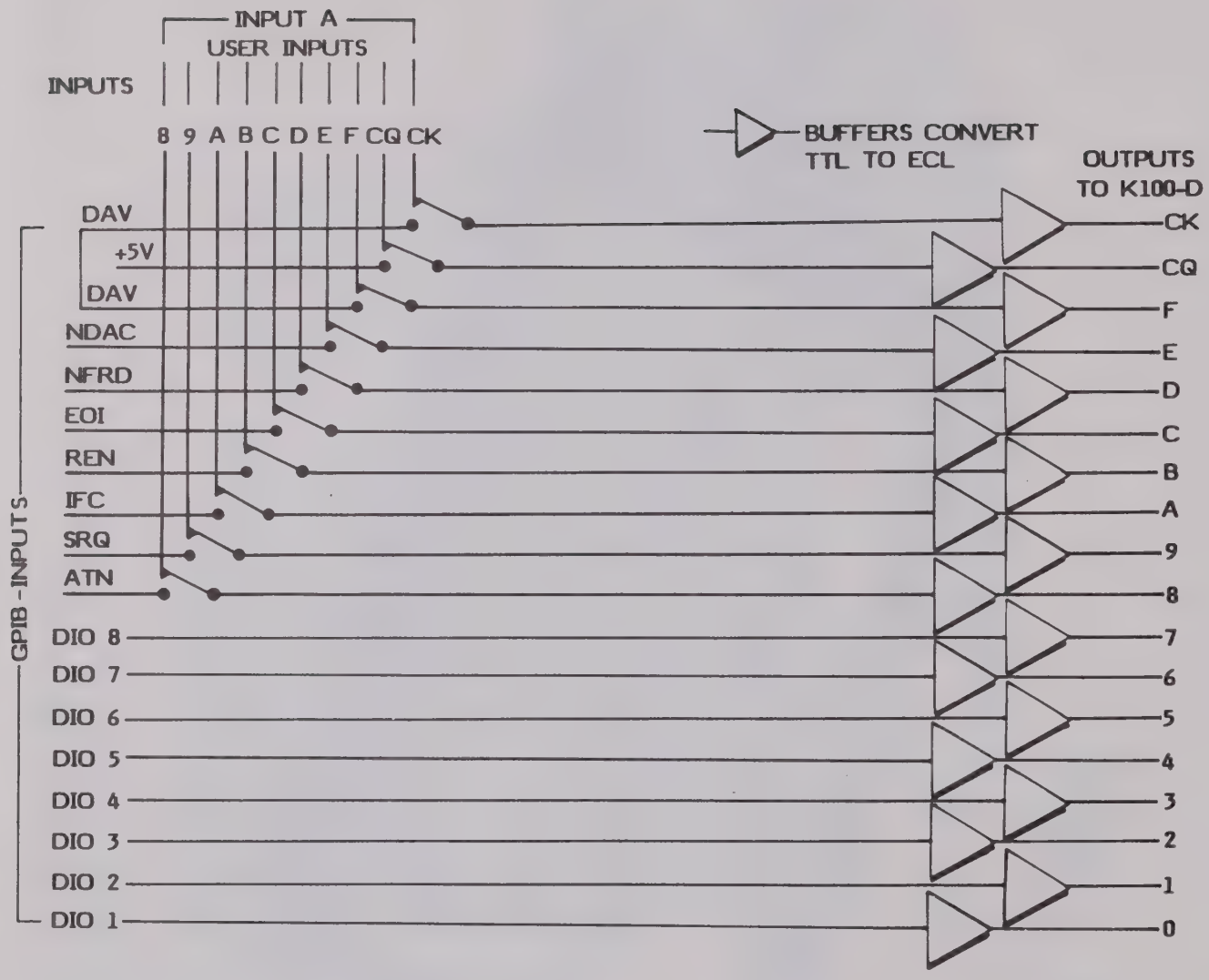

Figure 1.3 The Block Diagram of K100-D/488 GPIB Analyzer is shown with all switches in the user selected input positions. General management/handshake lines are not monitored.

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SECTION II

INSTALLATION

2.1 Introduction

This section contains information on unpacking, inspection, repacking, storage, and installation of the Model K100-D/488 GPIB Analyzer.

2.2 Unpacking and Inspection

Inspect instrument for shipping damage as soon as it is unpacked. Check for broken grabbers and connectors; inspect cables and panel surfaces for dents, scratches, and breaks. If the instrument is damaged in any way or fails to operate properly, notify the carrier immediately. For assistance of any kind, including help with instruments under warranty, contact your local Gould Inc., Instruments Division, Biomation Operation representative or Gould Inc., Instruments Division, Biomation Operation, in Santa Clara, California, U.S.A.

2.3 Storage and Shipment

To protect valuable electronic equipment during storage or shipment, always use the best packaging methods available. Contract packaging companies in many cities can provide dependable custom packaging on short notice.

2.4 Preparation For Use

2.4.1 Connect power to the pod via the $\pm$5.0 V output on the rear panel on the Model K100-D Logic Analyzer.

2.4.2 Plug the GPIB input cable (with connector labeled 488 INPUT), onto the edge connector closer to the top of the pod. Plug the user input cable (with connector labeled INPUT A), to the edge connector closer to the bottom of the K100-D/488. (See Figure 1.1).

2.4.3 Connect the other end of the GPIB (24 conductor) cable, via its "piggy-back" type connector (standard GPIB), to the system or instrument to be tested.

2.4.4 Connect the other end of the user input cable to test points as desired.

2.4.5 Connect the two large cables (hardwired to the pod) to the appropriate inputs on the lower right side of the front panel of the K100-D.

2.4.6 Put the appropriate user input switches in the user input positions for those lines selected as user inputs only. When all switches are in the GPIB position, all 16 GPIB lines can be monitored by the K100-D.

The K100-D/488 is now ready for use.

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SECTION III

OPERATION

3.1 Introduction

This section explains the use and function of the switches on the Model K100-D/488 GPIB Analyzer, as well as providing a typical application to familiarize the user with the operation of the Pod.

3.2 Controls and Capabilities

The K100-D/488 allows the user to conveniently view the 8 DIO (data lines) and 8 general management/handshake lines that comprise the 16 active lines of the GPIB. Ten switches (see Figure 1.2) are provided to allow the user to view non-GPIB data in lieu of the 8 handshake/management lines. When the 10 switches are in the GPIB INPUT position, all 16 active lines of the GPIB are viewed by the Model K100-D Logic Analyzer. The user can view non-GPIB inputs by putting the appropriate switch(es) in the USER INPUT position (see Figure 1.3). Note that two additional lines should be considered: When in the GPIB INPUT POSITION, (the Clock Qualifier) CQ input to the K100-D is tied to a (logic) true input (+5.0 V) and the Clock (CK) to the DAV line (Data Valid) from the GPIB under test. The K100-D can clock using non-GPIB originating signals by switching channels CK and CQ to the USER INPUT switch position. The user can view the phase relationship of the handshake signals by using a clock(s) derived from the system and synchronous to DAV but at a much higher frequency. Alternately, the user can view these phase relationships by utilizing the internal clock provided in the K100-D for asynchronous viewing. Again, the clock frequency should be much higher than that of DAV.

User inputs are input via the connector/cable labeled INPUT A (gray). The cable is terminated by 20 wire wrap receptacles. The black shielded receptacles are ground. The blue shielded receptacles are labeled with their corresponding K100-D channels, Clock (CK) and Clock Qualifier(CQ).

Open user inputs to the K100-D/488 will float high (TTL "1"). Although it appears possible to program channel threshold voltages, this feature is in fact disabled as the K100-D/488 inputs are referenced to a TTL threshold. Threshold settings on the K100-D status display have no effect on the K100-D/488.

3.3 Typical Applications

It is assumed that the user of K100-D/488 is familiar with the IEEE-std-488-1978 which is available from IEEE Incorporated, East 47th Street, New York, NY 10017. The user will probably be involved with the development of a GPIB interface to an instrument, or the creation of an entire GPIB based system, including several instruments.

For the instrument designer, the K100-D/488 can help in ascertaining if the instrument interfaces with the bus in the appropriate manner. For example; the designer may find that the data onto the bus from his instrument is not the same as appears on the display of the instrument's front panel. In addition, the data being output on to the bus changes although the instrument's display is not changing.

First, using the K100-D/488 set-up (see Section 3.2), the user monitors the data lines (DIO1-8) using DAV as the clock input to verify that the controller is seeing the same data as the logic analyzer and is functioning properly.

Second, the user inspects the timing relationship of the data (DIO1-8) and the DAV line by asynchronous clocking via the internal clock in the K100-D. He selects a time base at least 10X the frequency of DAV. The designer may find that DAV is TRUE before the data has settled. If that is not the source of the problem, he may try a third solution.

Third, the user inspects the timing relationship of DAV, NFRD, NDAC and the data (DIO-7). This is achieved using the internal clock of the K100-D, with a time base much greater than the rate of DAV (10X minimum). Triggering on NFRD, NDAC, or DAV using a delay allows a clear viewing of the timing relationships as shown in Figure 3.1.

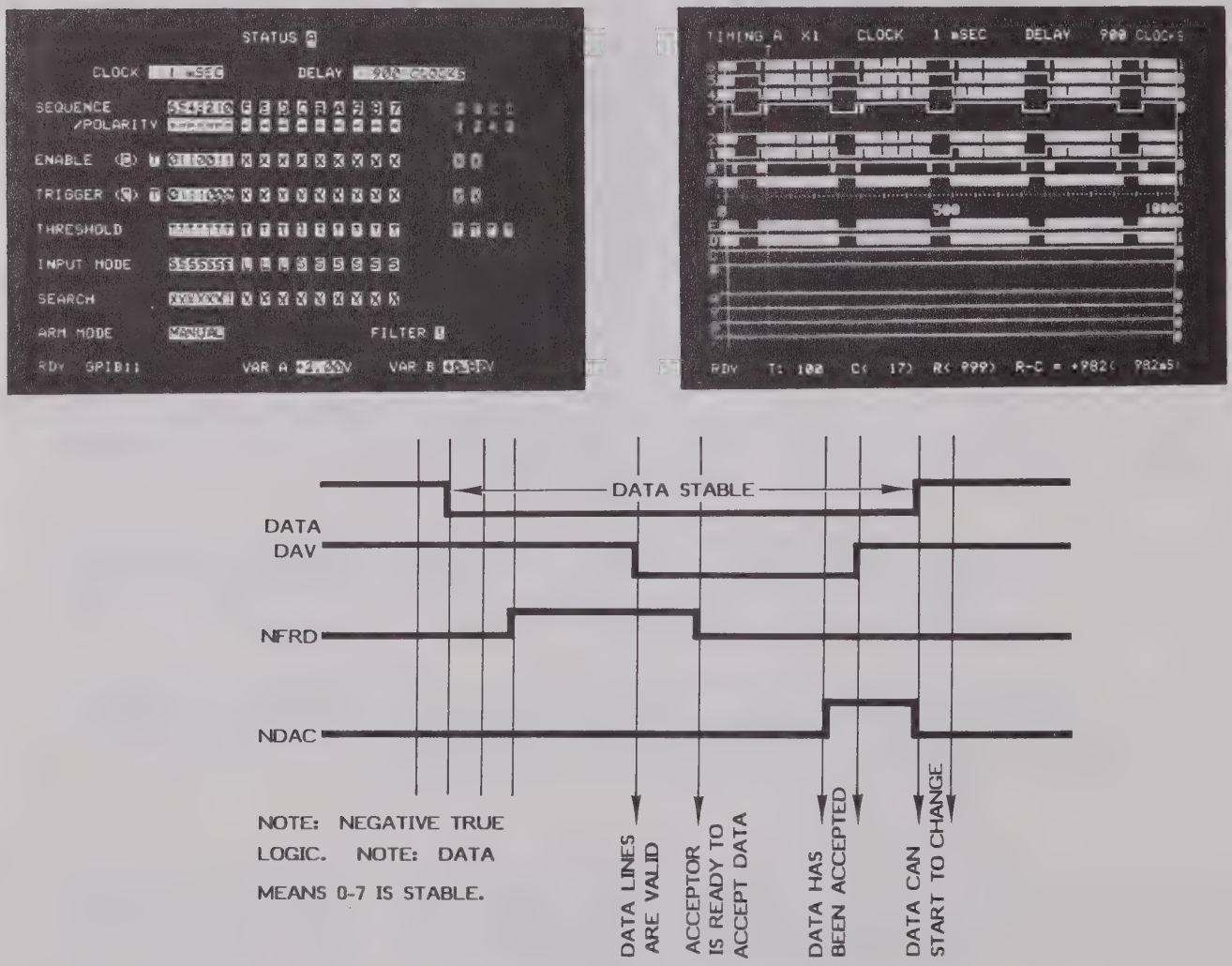

Figure 3.1 This is the timing diagram that can be expected when recording the handshake and data lines on the GPIB. The K100-D used asynchronous (internal) clocking at a rate high enough to allow at least 10 samples while NADC was high.

CHANNEL F is DAV
CHANNEL E is NDAC
CHANNEL D is NRFD
CHANNELS 0 to 6 are data lines

Many more steps may be required before the interface is completely debugged. The purpose of this text is to demonstrate a few examples.

The system designer may use the K100-D/488 to find out why the various bus compatible instruments he thought would interact properly are not doing so. The designer can view portions of programs by triggering on a particular instrument's talk address, after enabling on a previous talk address, where the two addresses are found sequentially in the program. The data streams can be checked for glitches (extremely short spikes) by running the program with the K100-D in the sample mode, entering the data into the B memory, then running the same program again with the K100-D in the latch mode, and then comparing memory A to B. All differences shown in the compare mode are the glitches.

It is possible that the IEEE-488 cable has had glitches induced on it by virtue of its physical placement near a high voltage spike source.

Glitch hunting is but one of the many uses the system designer may have for the K100-D/488. The user specified inputs allow the system designer to look inside his various instruments and determine which instrument, for example, is last to release the bus NDAC line. This is accomplished by looking at the source of the bus NDAC signal in a particular instrument prior to it being buffered onto the bus. That signal is compared to the bus NDAC line, and can be viewed in the portion of the program that has been deemed "slow" by the system designer.

Combined with the K100-D/488, the K100-D is a highly flexible tool for bus analysis. It's uses go far beyond the applications outlined here. Our application engineering staff is available to discuss applications with you.

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SECTION IV

THEORY OF OPERATION

4.1 Introduction

The Model K100-D/488 GPIB Analyzer is designed as a passive interface device to monitor a GPIB IEEE 488 bus.

4.2 Functional Description

The 488 pod allows the user to monitor an IEEE-488-1975 standard, or allows the user to monitor any TTL logic family using the "User Input" cable assembly.

4.3 Functional Detail

The user can either select the IEEE 488 input, or the user input, which is selected through double pull, double throw switches which protrude through the case of the pod. Once the signals have been selected, the 488 pod uses level translators to translate the data input from the TTL Logic family to the ECL logic family for transmission into the K100-D.

The output of the 488 pod (Input A, B) are routed through flat ribbon cables in paired differential ECL signals to the Model K100-D Logic Analyzer for noise immunities.

NOTE: The output of the 488 pod is unterminated differential ECL for each signal that goes into the K100-D. The termination is in the K100-D on the front-end board.

The 488 pod receives its power through a LEMO connector which is connected to the rear panel of the K100-D; this LEMO connector supplies ± 5 V and a logic ground. The LED indicates that power is applied to the 488 pod.

4.4 Detailed Description

The IEEE 488 bus monitoring is received on the 488 pod through a resistive network which presents a load to the device of approximately 2 k Ω, and a voltage reference of approximately 3.37 V. This is a Thevinin equivalent of the 3.9 to 5 V and the 6.2 to ground. These are the IEEE standard termination values. The GAB and GAC, NRFD, et cetera to DI01. All these lines are terminated per the standard using the resistive network pack, RP1 and RP2.

The path through the IEEE standard, once received into the pod, is terminated and driven through 74 LS244 tri-state devices. These devices are always enabled by attaching pins 1 and 19 to ground. Therefore, they are used for buffering to provide a high impedance, low power source to the GPIB bus, which is also the IEEE standard. The signals are routed to the level translators via switches S pack 1 and S pack 2.

These signals either allow the IEEE 488 to be routed to the level translators or the user port input (J4-2 to J4-20 respectively).

The IEEE 488 path continues through from the connector, through the termination, through the buffer, through the S packs, and goes to a 10 124 logic device which is a TTL to ECL translator. The translator will translate the voltages from the TTL logic level to the ECL logic level for differential transmission to the K100-D.

NOTE: **Lines 0, 1, 2, on up to channel F, these logic levels will go into the K100-D through ribbon cables and connectors input A and input B, to be displayed on the K100-D with the same format. Channel 0 being channel 0 on the K100-D; channel F being channel F on the K100-D.**

The other path that you can follow into the K100-D/488 pod is through the user's port option. This is a flying lead input connection which means the cable can be connected to the IC sockets or a clip to look at two TTL logic families. The lines on the J4 connector are loaded with the high impedance, low power LS-244 devices, which are always enabled through pins 1 and 19. These signals are routed to connections on the K100-D, 8 through F, CQ, and clock via switch pack 1 and switch pack 2.

To summarize, the IEEE 488 pod is used to monitor either logic families, or TTL, or the logic TTL under both standards of the IEEE 488 1975, and is essentially a bit switch to input either the GPIB, or the user's port, to the K100-D as shown in the block diagram (Figure 1.3).

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SECTION V

CALIBRATION PROCEDURES

5.1 Recalibration of Internal Circuits

There is no calibration of the internal circuitry of the Model K100-D/488 GPIB Analyzer.

5.2 Required Test Equipment

The following test equipment are required to verify performance of the K100-D/488.

1. 250 MHz Oscilloscope; two channels with horizontal resolution to 1 ns (Tektronix 475A).

2. Pulse generator (Tektronix PG502 or equivalent).

3. Model K100-D Digital Logic Analyzer.

5.3 Power Supply Verification

Remove the top and bottom covers of the unit via four screws located on the bottom cover. Plug in the power cable connector into the rear of the K100-D and verify that +5.0 VDC and -5.2 VDC are present at the P.C.B. Red wire is +5.0 V, Black wire is ground, and Green wire is -5.2 V.

Voltage	Range
+5.0 VDC	±50 mV
-5.2 VDC	±50 mV

Verify that the voltages are within the range specified and that the green power LED is lit.

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SECTION VI

MAINTENANCE

6.1 Introduction

This section covers the Model K100-D/488 GPIB Analyzer diagnostic routine. Repair of the board can be performed with the aid of the technical description in Section IV as well as the diagnostic routine in this section.

The drawings in Section VII have been included to aid service personnel who wish to troubleshoot to the component level. Additional assistance regarding a particular problem can be obtained by contacting the Customer Service Department at the factory: Phone (408) 988-6800, TWX 910-338-0509.

6.2 Functional Checkout

The following procedure checks the operation of all channels of the GPIB Analyzer.

6.2.1 Connect the K100-D/488 output cables to their respective connector, A and B inputs, on the front panel of the K100-D.

6.2.2 Plug in the LEMO power cable connector into the rear of the K100-D and turn it's power switch ON.

6.2.3 Turn on the pulse generator and adjust the output of 1 MHz square-waves at TTL levels (0.0 V to approximately 4.0 V amplitude).

NOTE: Connection of the signal generator output to the GPIB inputs of the pod may be accomplished in one of two ways. Either inject the square-waves at the J1 edge-connector fingers of the P.C.B. with suitable 26-pin card-edge connector, or use a mating connector for the GPIB 24-pin connector P1 on the GPIB input cable. Connection of the square-wave generator output to the USER INPUT port may be accomplished by either using the "push-on" wire wrap receptacles at the user input cable, or by using a suitable 20-pin card-edge connector (0.1" centers).

6.2.4 Connect the square-wave signal generator output to GPIB input connector J1-1(DIO1). Connect up generator ground to one of the card-edge connector grounds J1-12, 14, 16, et cetera. With the K100-D in status mode and power-up complete, the combinational trigger word will be all don't cares (X's) except for a 1 for channel 0. Press [AUTO ARM] switch, then [TIMING]. Verify that signal is being recorded and displayed on channel 0.

6.2.5 Disconnect signal from J1-1 (DIO1) and connect it to J1-3 (DIO2). Press [STATUS] , [TRIGGER] , [X] (14 times), [1] , [X] , [ENTER] , [AUTO ARM]. Press [TIMING] . Verify that signal is present on channel 1.

6.2.6 Remove signal at J1-3 (DIO2) and connect to J1-5 (DIO3). Press [STATUS], [TRIGGER] , [X] (13 times), [1] , [X] , [X] , [ENTER] , [AUTO ARM] , [TIMING] . Verify signal on channel 2.

6.2.7 Remove signal at J1-5 (DIO3) and connect to J1-7 (DIO4). Change trigger to all X's except 1 for channel 3. [AUTO ARM], [TIMING]. Verify signal on channel 3.

6.2.8 Remove signal at J1-5 (DIO3) and connect to J1-2 (DIO5). Change trigger accordingly. Press [AUTO ARM] , [TIMING] . Verify signal on channel 4.

6.2.9 Remove signal at J1-2 (DIO5) and connect to J1-4 (DIO6). Change trigger accordingly. Press [AUTO ARM] , [TIMING] . Verify signal on channel 5.

6.2.10 Remove signal at J1-4 (DIO6) and connect to J1-6 (DIO7). Change tigger accordingly. Press [AUTO ARM] ,[TIMING] . Verify signal on channel 6.

6.2.11 Remove signal at J1-6 (DIO7) and connect to J1-8 (DIO8). Change trigger accordingly. Press [AUTO ARM] , [TIMING] . Verify signal on channel 7.

6.2.12 Remove signal at J1-8 (DIO8). Now connect up all 10 channels of the USER INPUT port to the generator by using the input cable "push-on" wire wrap receptacles or a card-edge connector. Connect the signals to a common tie-point and to the square-wave generator, and tie the grounds together and to the generator ground.

6.2.13 Flip all of the GPIB Analyzer switches to the USER INPUT position. Press [STATUS] , [TRIGGER] , [F] (4 times), [AUTO ARM], [TIMING]. Verify that channels 8 through F are displaying square-waves. Check that channels CK and CQ are active by monitoring the respective outputs of the ECL 10124 TTL-to-ECL translator 1A. Use an oscilloscope to do this. Refer to schematic and assembly drawings listed in Section VII.

6.2.14 Flip all of the GPIB Analyzer switches to the GPIB Input position. Press [AUTO ARM] , [TIMING] , [M→A] . Verify that all channels 8 through F are high (logic 1).

This completes the functional check of the K100-D/488 adapter.

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SECTION VII

SCHEMATICS AND ASSEMBLY DRAWINGS

7.1 Introduction

This section contains the schematics and assembly drawings for the Model K100-D/488 GPIB Analyzer. Parts lists are also included for user convenience.

7.2 List of Drawings

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7.3 Parts Lists

The materials in the following lists are subject to change without Gould Inc.'s prior notification. For list verification, contact the Customer Service Department at the factory: Phone (408) 988-6800, TWX 910-338-0509.

7.3.1 List of Parts List

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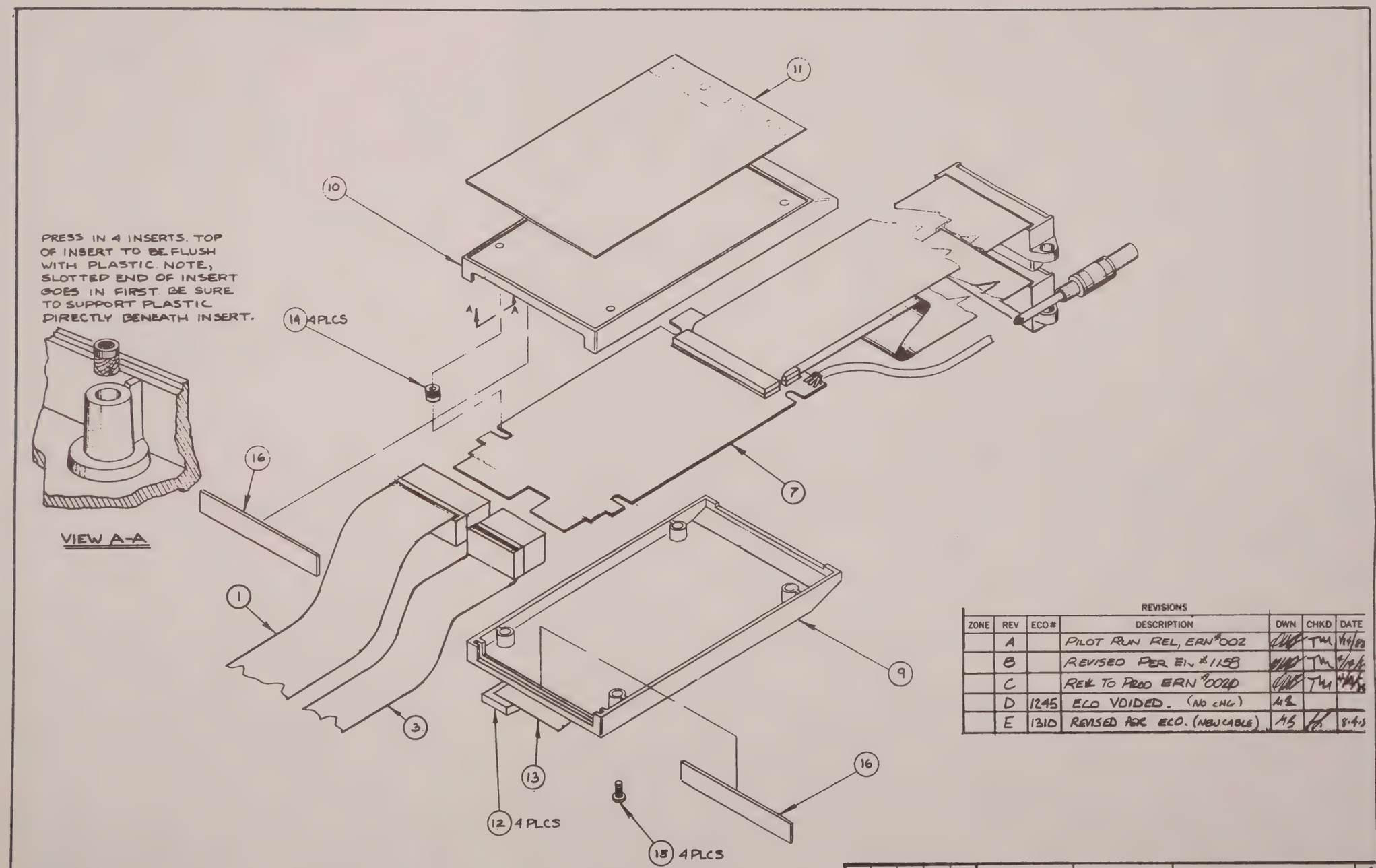


REVISIONS

ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT RUN REL, ERN#002		TM	11/1/79
	B		REVISED PER ECN #1158		TM	1/14/80
	C		REL TO PROD ERN#002D		TM	4/24/80
	D	1245	ECO VOIDED. (NO CHG)	MS		
	E	1310	REVISED PER ECO. (NEW CABLE)	MS		8-4-83

DASH NO.	NUMBER	QTY
-10	0112-0164	1
	NEXT ASSEMBLY	

-50 -40 -30 -20 -10 | PART NUMBER | PART NAME | DESCRIPTION/SPECIFICATION | ITE

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± 1 ANGLES .XX ± .020 ± 1° .XXX ± .010

HOLE SIZE .0-.500 ± .003 .000-.999 ± .004 1.000-1.499 ± .005

ENG. SERV. RG DATE 1/23/80

	DRAWN	DATE
	DRS	7-18-79
CHECKED	TMC	1/14/80
PROJ. ENG.	Curt	1/23/80
MANUFACTURING		1/23/80
QUALITY ASSUR.		1/23/80

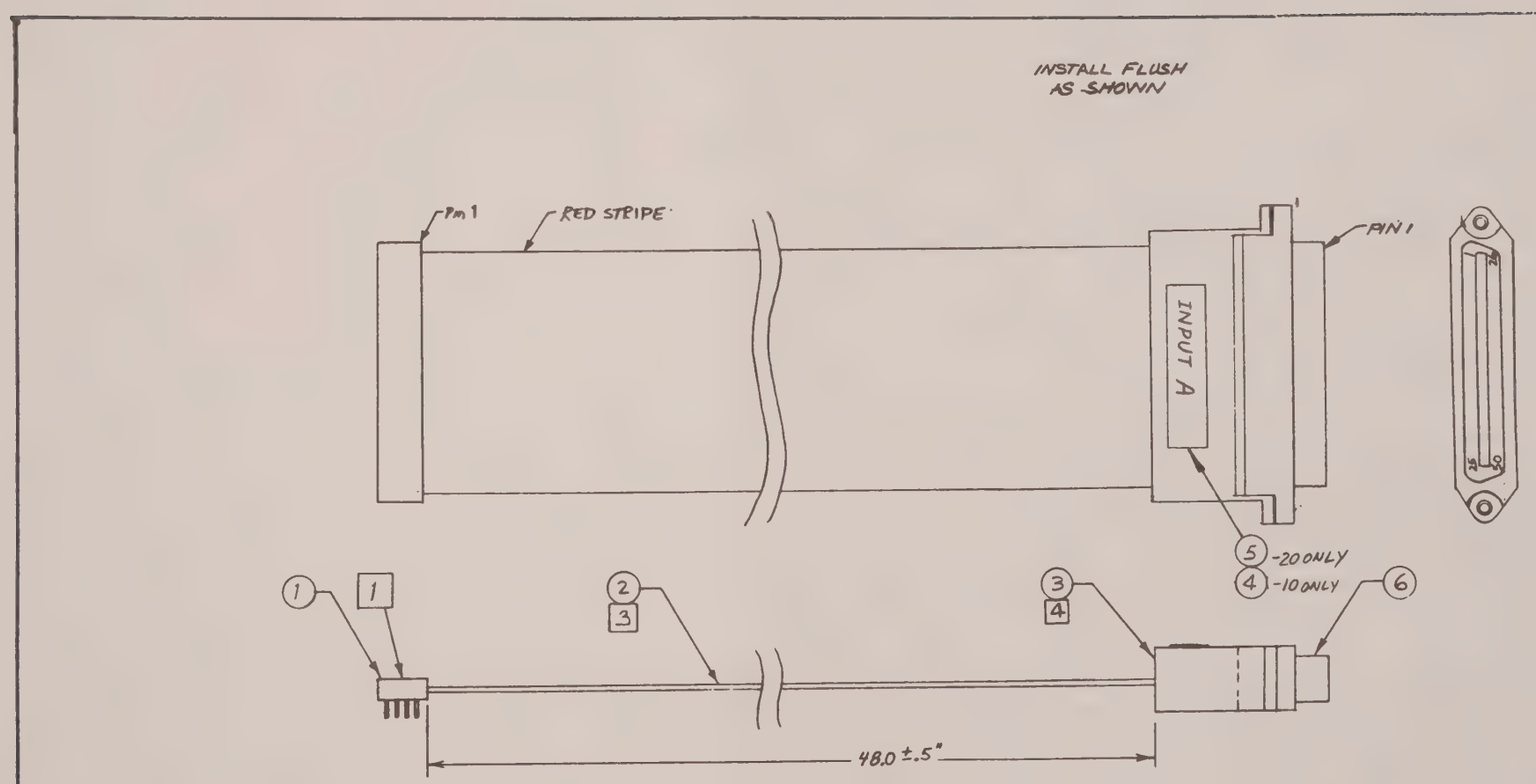
GOULD biomation

TITLE: TOP ASSEMBLY K100/488

SCALE	SIZE	PART NUMBER
NONE	C	0112-0100

CODE | SHEET 1 OF 1

Figure 7.1



-10 ASSY SHOWN
(-20 ASSY SIMILAR EXCEPT AS NOTED)

REV -: PILOT RUN RELEASE

REV A: REVISED PER ECO N° 0712
3-19-79 RUSSELL TM

REV B: INCORP. ECO N° 0740
3-19-79 RUSSELL TM

(REV B) RELEASED FOR PRODUCTION
PER EN # 1031 6-6-79 SWL

REV C: REVISED PER ECO N° 0848
J CARROLL 7-17-79

REV D: REVISED PER ECO N° 0956
J Carroll 10-18-79 TM

NOTES:

1. MARK WITH PART NO. 0112-0131 AND REVISION LEVEL IN AREA SHOWN, USING 1/8" BLACK CHARACTERS.
2. SEE SHEET 2 FOR HOOK-UP CONFIGURATION.
3. CABLE TO BE FREE OF VENDOR OR MANUFACTURE'S IDENTIFICATION.
4. INSTALL BACKSHELL WITH SUPPLIED PIN AFTER TERMINATING CABLE AT CONNECTOR.

DASH NO.	NUMBER	QTY
	NEXT ASSEMBLY	
-20	0112-0185-20	1
-10	0112-0185-10	1

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS √
TOLERANCE
DIMENSIONAL: X ± 1 ANGLES; XX ± .020 ± 1°; XXX ± .010
HOLE SIZE: 0 .500 ± .003; .600 .999 ± .004; 1.000 1.499 ± .005
BEND RADIUS
FINISH

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM
								3
								2
								1

DRAWN	C BLANDING	DATE 11/27/78
CHECKED	TM McCann	11/28/78
ENGINEER	C Blanding	11/30/78
MANUFACTURING	K Nagel	12/4/79
QUALITY		

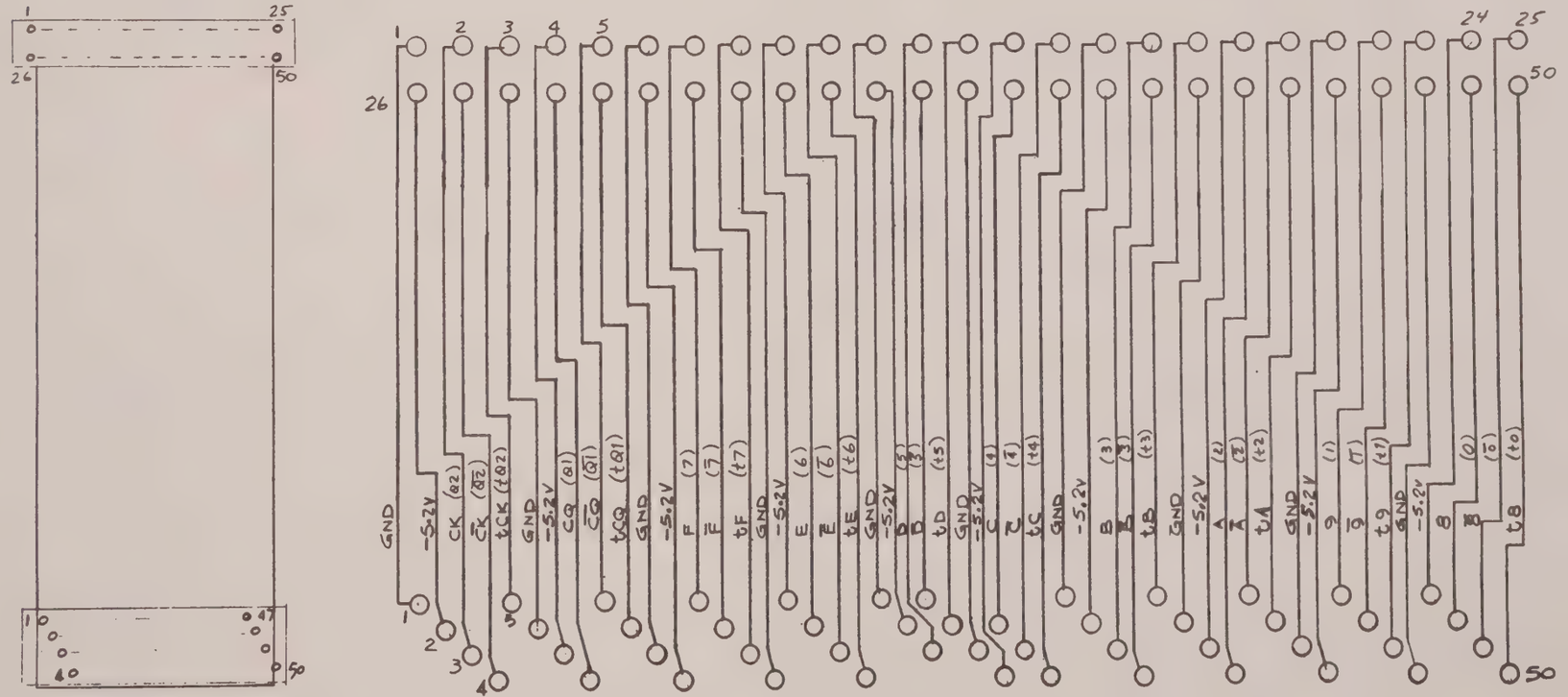
GOULD biomation

TITLE: ASSEMBLY - OUTPUT CABLE

SCALE	SIZE	PART NUMBER	REV
—	C	0112-0131	D

CODE K1000 SHEET 1 OF 2

Figure 7.2



NOTES:

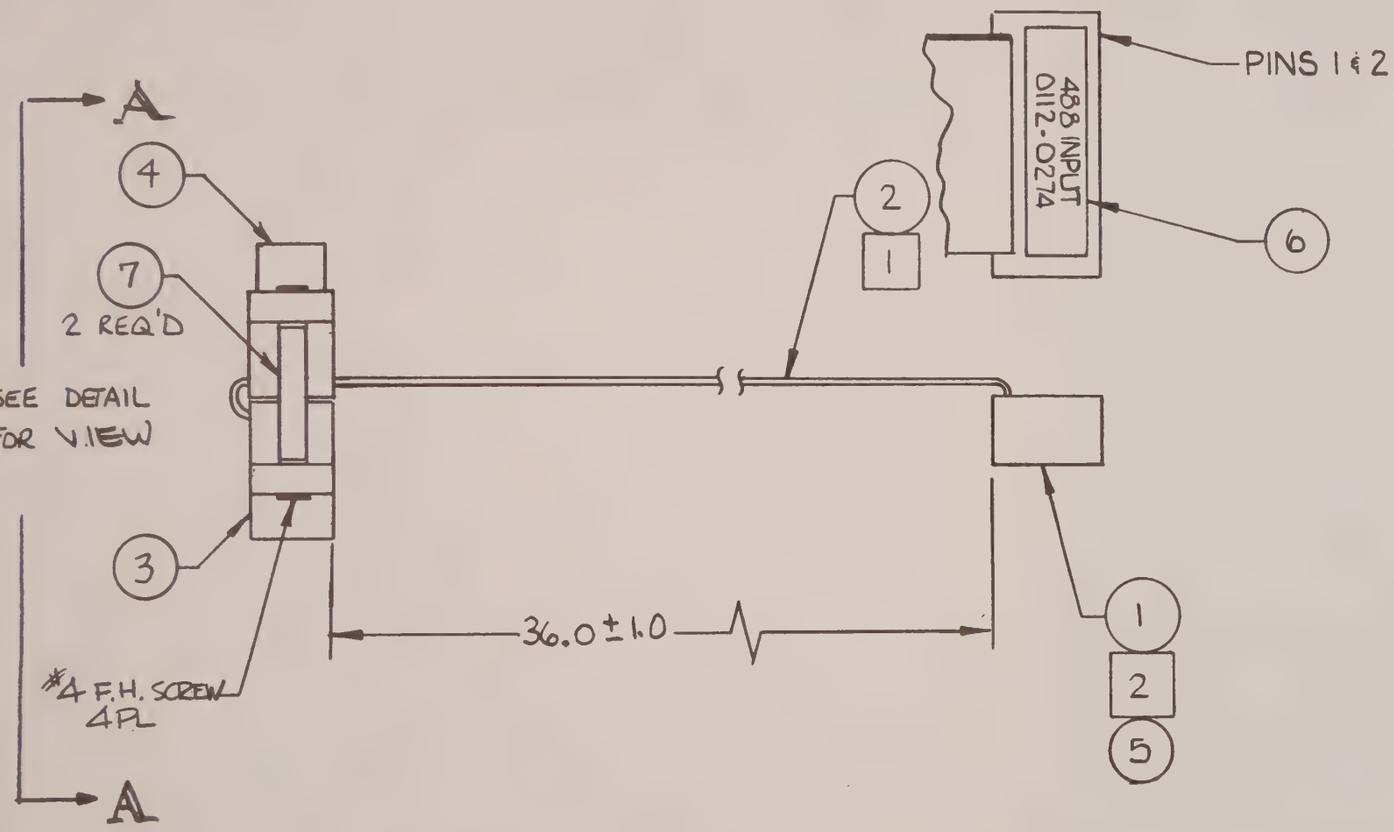
1. SIGNAL NAMES SHOWN ARE FOR REFERENCE ONLY
-20 ARE IN PARENTHESIS.

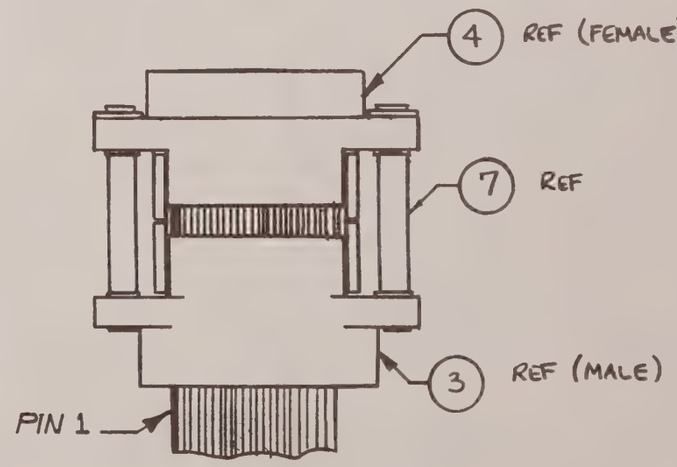
			3
			2
			1
PART NUMBER	PART NAME	DESCRIPTION SPECIFICATION	ITEM

DRAWN	DATE	GOULD biomation	
CHECKED		TITLE ASSEMBLY OUTPUT CABLE	
ENGINEER			
MANUFACTURING		SCALE — / SIZE C / PART NUMBER 0112-0131	REV D
QUALITY ASSUR		CODE K100D	SHEET 2 OF 2

Figure 7.3

REVISIONS					
REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
A		PILOT RELEASE ERN 002	CR	TM	1/11/80
B		REVISED PER EN 1161	MB		
C		RELEASED TO PROD. PER ERN #0021	MB		
D		REVISED PER E.C.O # 1272	JWC	RP	8-5-80





VIEW A-A

NOTES:

1. REMOVE 25TH & 26TH CONDUCTORS FROM CABLE PRIOR TO ASSEMBLY.
2. KEY INSERTED BETWEEN LOCATIONS 19/20 & 21/22
3. CONNECT PIN 1 OF ALL CONNECTORS TO THE SAME WIRE.

-50	-40	-30	-20	-10	PART NUMBER	PART NAME	DESCRIPTION/SPECIFICATION	ITEM
								1

DASH NO.	NUMBER	QTY
-01	0112-0160	1
	NEXT ASSEMBLY	

DO NOT SCALE DRAWING

REMOVE ALL BURRS AND SHARP EDGES. DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT. SURFACE ROUGHNESS

TOLERANCE

DIMENSIONAL: X ± .1 ANGLES .XX ± .020 ± 1° .XXX ± .010

HOLE SIZE: .0-.599 ± .003 .600-.999 ± .004 1.000-1.499 ± .005

ENG. SERV.	RG	DATE 4/23/80
DRAWN	C Rasmussen	DATE 7-10-79
CHECKED	T McCann	4-23-80
PROJ. ENG.	Curt	1-14-80
MANUFACTURING	M Gould	4/23/80
QUALITY ASSUR.	K Hawkins	4/23/80

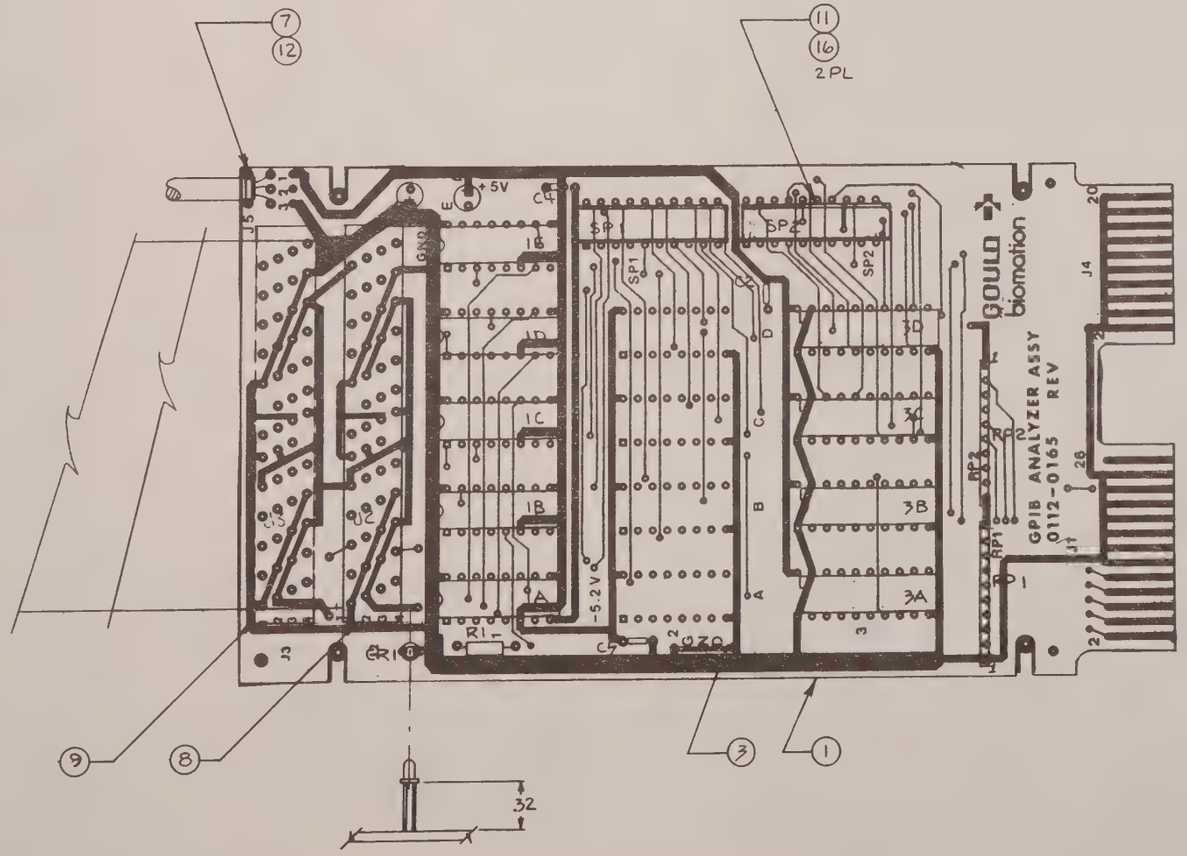
GOULD biomation

TITLE: CABLE, GPIB ANALYZER

SCALE	SIZE	PART NUMBER	REV
1/1	B	0112-0274	D

CODE | SHEET 1 OF 1

REVISIONS						
ZONE	REV	ECO#	DESCRIPTION	DWN	CHKD	DATE
	A		PILOT RUN REL ERN 002	JW	TM	
	B		REVISED PER EN #1151		TM	
	C		REVISED PER EN 1155		TM	
	D		REL TO PROD ERN 0021		TM	
	E		REVISED PER ECO# 1288	LD	RD	
	F		REVISED PER ECO#1291	LD	RD	
	G	1390	REVISED PER ECO.	MB		



| | | | | | |

P1
DIO1 -1
DIO5 -2
DIO2 -3
DIO6 -4
DIO3 -5
DIO7 -6
DIO4 -7
DIO8 -8
EOI -9
REN -10
DAV -11
GND -12
NRFD -13
GND -14
NDAC -15
GND -16
IFC -17
GND -18
SRQ -19
GND -20
ATN -21
GND -22
SHIELD -23
GND -24
-25
-26

J1 - 1
- 2
- 3
- 4
- 5
- 6
- 7
- 8
- 9
- 10
- 11
- 12
- 13
- 14
- 15
- 16
- 17
- 18
- 19
- 20
- 21
- 22
- 23
- 24
- 25
J1 -26

DAV
NDAC
NRFD
EOI
REN
IFC
SRQ
ATN
DIO8
DIO7
DIO6
DIO5
DIO4
DIO3
DIO2
DIO1

3.0K 6.2K
RP2
RP1

+5V

74LS244

SP2
SP1
+5V

1B 10124
1C 10124
1D 10124
1E 10124

F F E E D D C C B B A A 9 9 8 8 7 7 6 6 5 5 4 4 3 3 2 2 1 1 0 0

J2 -13
-14
-18
-19
-23
-28
-29
-33
-34
-38
-39
-43
-44
J3 -48
J3 -49

INPUT A
INPUT B

J5
C1 47/16
C2 .1
C3 47/16
C4 .1
C5 .1
+5V
-5.2V

SP2
+5V

1A 10124

CK CK CQ CQ Q2 Q2 Q1 Q1

J2 - 3
J2 - 4
J2 - 8
J2 - 9
J3 - 3
J3 - 4
J3 - 8
J3 - 9

INPUT A
INPUT B

R1 300
GRN
CR1
+5V

J4 - 2 CK
J4 - 1
- 4 CQ
J4 - 3
- 6 F
J4 - 5
- 8 E
J4 - 7
- 10 D
J4 - 9
- 12 C
J4 - 11
- 14 B
J4 - 13
- 16 A
J4 - 15
- 18 9
J4 - 17
- 20 8
J4 - 19

3D 3A

74LS244

GND:
J2 - 1, 6, 11, 16, 21, 26, 31, 36, 41, 46
J3 - 1, 6, 11, 16, 21, 26, 31, 36, 41, 46

-5.2V:
J2 - 2, 7, 12, 17, 22, 27, 32, 37, 42, 47
J3 - 2, 7, 12, 17, 22, 27, 32, 37, 42, 47

J2 → INPUT A CK, CQ, F-8

J3 → INPUT B Q2, Q1, 7-0

REVISIONS				
REV	DESCRIPTION	BY	DATE	APPD
A	PILOT RUN REL, ERN 002			TM
B	REVISED PER EN#1151			
C	REVISED PER EN#1155			TM
D	REL TO PROD PER ERN 0021		2ND	TM

50 -40 30 -20 -10 | PART NUMBER | PART NAME | DESCRIPTION SPECIFICATION | ITEM

DO NOT SCALE DRAWING
REMOVE ALL BURRS AND SHARP EDGES
DIMENSIONS ARE IN INCHES AND APPLY OVER ADDED FINISHES EXCEPT PAINT
SURFACE ROUGHNESS √
TOLERANCE
DIMENSIONAL
X ± .030 ±1
XX ± .010
HOLE SIZE
0 TO .500 ± .003
.501 TO .999 ± .004
1.000 TO 3.000 ± .005
BEND RADIUS
FINISH

DRAWN C. Blamby DATE 7-24-79
CHECKED
ENGINEER 1-1-80
MANUFACTURING 4-23-80
4/23/80

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TITLE SCHEMATIC - K1000/488 GPIB ANALYZER
SCALE —
SIZE D
PART NUMBER 0112-0166
REV D
CODE
SHEET 1 OF 1

DASH NO | NUMBER | QTY | NEXT ASSEMBLY

Figure 7.6

ITEM	QUANTITY PER ASSEMBLY						PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
	-60	-50	-40	-30	-20	-10						
1						1	0112-0274	CABLE, GPIB, INPUT				LM
2												
3						1	0112-0365-30	CABLE, USER INPUT			INPUT A	LM
4												
5												
6												
7						1	0112-0165	PCB ASSY				LM
8												
9						1	0112-0071-10	CASE, BOT				
10						1	0112-0300	CASE, TOP				
11						1	0112-0161	PANEL				
12						4	7000-0243	FOOT				
13						1	0610-0032	SERIAL TAG				
14						4	7000-0269	INSERT				
15						4	7000-0384	SCREW				
16						2	0112-0141	FRONT PNL				
17												
18												

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	REL TO PILOT RUN ERN 002	1/10/80		TM	
B	REVISED PER EN # 1158	4/19/80		TM	
C	REL TO PROD ERN 0021	4/23/80		TM	
D	ECO # 1245 VOIDED. (NO CHG)	8.4.80	AB		
E	ECO # 1310 NEW CABLE ASSY.	8.4.80	AB		

DASH NO.	NUMBER	QTY
-10	0112-0164	1
	NEXT ASSEMBLY	

		DATE
DRAWN	CKasmyasm	7-17-79
CHECKED	Mc Cann	4-23-80
ENGINEER	Curt	4-23-80
MANUFACTURING		4/23/80
QUALITY ASSURANCE		4/23/80

LIST OF MATERIAL
TOP
ASSEMBLY
K100/488

MODEL K100D

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REV		REV
B	0112-0160	E

CODE | SHEET 1 OF 1

Figure 7.7

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1						1	0112-0167	PWB				
2												
3						1	9000-0054	BUSS WIRE FORMED				
4												
5						4	1800-0240	I C	3A-3D	OCTAL BUFFER	74LS244	
6						5	1850-0021	I C	1A-1E	QUAD TTL→ECL	10124	
7						1	0010-0055	CABLE, PWR				LM
8						1	0112-0131-10	K100 INPUT A				LM
9						1	0112-0131-20	K100 INPUT B				LM
10						2	3700-0049	RES PACK	RP1, 2	10PIN SIP	3K/6.2K	
11						2	6600-0115	SW PACK	SP1, 2			
12						1	7200-0025	MOUSE TAIL				
13						1	6400-0041	DIODE, LED	CR1		GREEN	
14						2	4300-0025	CAPACITOR	C1,3		47/6V	
15						3	4000-0025	↓	C2,4,5		.1µF	
16						2	6100-0121	SOCKET, SW	(SP1, 2)		20 pin	
17						1	3000-3000	RESISTOR	R1		300Ω, 1/4, ±5%	
18												

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
A	REL TO PILOT RUN PER ERN 002	8-21	JW	JM	
B	REVISED PER EN #1151	3/12			
C	REVISED PER EN #1155	4/11			
D	REL TO PROD ERN 0021	4/23		YM	4/23/80
E	REVISED PER E.C.O #1288	7-30		RO	
F	REVISED PER ECO #1291	7-30		RO	
G	REVISED PER ECO #1390	3-24-81	MG		

DASH NO.	NUMBER	QTY
-10	0112-0160	1
	NEXT ASSEMBLY	

		DATE
DRAWN	J.E. WELDON	8-21-79
CHECKED	T. McLaurin	4-22-80
ENGINEER	Curt	4-23-80
MANUFACTURING	[illegible]	4/23/80
QUALITY ASSURANCE	[illegible]	4/23/80

LIST OF MATERIAL
ASSEMBLY
K100/488
GPIB ANALYZER

MODEL K100

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B	0112-0165	REV G
CODE		SHEET 1 OF 1

Figure 7.8

ITEM	QUANTITY PER ASSEMBLY -60	-50	-40	-30	-20	-10	PART NUMBER	PART NAME	REF. DESIGNATION	VENDOR NO.	DESCRIPTION	TYPE
1					1	1	6000-0106	CONNECTOR		3M 3426-0000T	50 PIN, PC MOUNT	
2					A/R	A/R	7100-0029	CABLE			50 COND., 28 AWG	
3					1	1	6000-0263	BACKSHELL				
4					—	1	0112-0142-01	LABEL	"INPUT A"			
5					1	—	0112-0142-02	LABEL	"INPUT B"			
6					1	1	6000-0262	CONNECTOR			50pin "AMP-CHAMP" TYPE	
7												
8												
9												
10												
11												
12												
13												
14												
15												
16												
17												
18												

REF. DRAWINGS

REV	DESCRIPTION	DATE	DWN	CKD	APPD
—	PILOT RUN RELEASE EN 0948	11/21/78	RS		
A	REVISED PER ECO Nº 0712	3-1979	RITCH	TM	
B	INCORP ECO Nº 0740	3-1979	RITCH	TM	
C	INCORP ECO Nº 0848	7-17-79	JC.		
D	REVISED PER ECO 956	10-18-79	JC.	TM	

DASH NO.	NUMBER	QTY
20	0112-0135-10	1
10	0112-0135-10	1
20	0112-0185-20	1
10	0112-0185-10	1

NEXT ASSEMBLY

		DATE
DRAWN	C. Blanding	10-10-78
CHECKED	Mc Cann	11-28-78
ENGINEER	C. Blanding	11-30-78
MANUFACTURING		1/10/79
QUALITY ASSURANCE		1/10/79

LIST OF MATERIAL

ASSEMBLY, OUTPUT CABLE

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MODEL K100D

B | 0112-0131 | REV D

CODE

SHEET 1 OF 1

Figure 7.9

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19050 Pruneridge Ave., Cupertino, CA 95014-0718
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